13.1 A 56mW CT Quadrature Cascaded ΣΔ Modulator with 77dB DR in a Near Zero-IF 20MHz Band

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Higher data-rates and increased digitization in wireless systems put more demands on the A/D converter in terms of bandwidth and dynamic range. Due to their power efficiency, ΣΔ A/D converters are widely used in wireless receivers. In the last few years, ΣΔ modulator designs are being pushed to achieve higher bandwidths and resolution [1, 2]. Exploiting the vast potential of ΣΔ modulation, a cascaded ΣΔ modulator with CT quadrature loop filters is proposed. The A/D converter has a DR of 77dB and 20MHz bandwidth at an IF of 10.5MHz. Moreover, it features inherent anti-aliasing filtering, and does not suffer from DC offset or 1/f noise, that are outside the near zero-IF (NZIF) signal band.

Figure 13.1.1 illustrates the block diagram of the A/D converter. It is a 2-stage cascaded ΣΔ modulator with quadrature loop filters. The first stage consists of the quadrature loop filter QLF1, A/D converters ADC1i and ADC1q, and feedback D/A converters DAC1i and DAC1q. The quantization error, Qi+jQq, of the first stage is obtained by feeding digital outputs Y1i and Y1q to D/A converters DAC2i and DAC2q, respectively, and subtracting their outputs from the inputs of ADC1i and ADC1q. This quantization-error signal, Qi+jQq, is then fed to a second cascaded stage comprising loop filter QLF2, A/D converters ADC2i and ADC2q, and D/A converters DAC3i and DAC3q. The digital outputs of the 2 stages both contain the quantization error Qi+jQq, but with different transfer functions. Therefore, the second stage output is fed to a digital quadrature noise-cancellation filter (QNCF) in order to match both transfer functions. Subtraction of the QNCF output from a delayed version of the first stage digital output cancels out Qi+jQq. The resulting signal Yi+jYq has very little quantization noise in the band of interest. Finally, a quadrature decimation filter (QDF) filters off the out-of-band quantization noise. A known issue of CT cascaded ΣΔ modulators is that the analog RC time constants of loop filters QLF1 and QLF2 vary due to process spread. To address this issue, a calibration loop is required. The calibration algorithm that is used to correct for RC spread is based on the method in [3], but in this design the analog loop-filter coefficients are calibrated rather than the coefficients of the digital QNCF. Therefore, the analog bandwidth is always correct after calibration.

Figure 13.1.2 shows a more detailed block diagram of the ΣΔ modulator. The 2-stage cascaded architecture has 2^{nd}-order CT quadrature loop filters. Each filter consists of 2 active-RC resonator sections with feedforward capacitors C2i/C2q and C5i/C5q for high-frequency stabilization. Resistor pairs R5i-R8i and R5q-R8q determine the locations of the noise transfer function (NTF) zeros. All NTF zeros are optimally placed in the 20MHz signal band around a +10.5MHz IF. Each resistor (except for R1i/R1q) is programmable within a range of approximately ±40% from the nominal value, with 1% accuracy. The schematic of the programmable (P+ Poly) resistors is shown in Fig. 13.1.3. It consists of a fixed resistance (Rc + Rf) and a coarse and fine programmable resistor arrangement, set by control bits D0-D4 and D5-D8, respectively. The switches have low impedances compared to resistors R0-R8 and are connected to the virtual-ground nodes of the OTA, that ensures high linearity. Note that due to the fact that the RC time-constant calibration is done with programmable resistors only, the thermal noise of the loop filter varies slightly, depending on the value of the actual capacitors.

All quantizers are 4b flash converters that comprise 15 comparators and a 15-taps resistive reference ladder. The thermometer output code of each quantizer is connected to a 4b SC DAC that consists of 15 unit cells. Because the charge is mainly at the beginning of the feedback pulse, the SC DAC can easily be delayed by half a clock period. This allows a sufficiently large time slot for the comparators to make a decision. The OTAs of the first resonator stage are biased with the largest currents, as they have to linearly handle peak currents of a few mA of the SC DACs. To save power, the bias currents of the OTAs in the other resonator stages are scaled down by a factor of 4. Each OTA is implemented as a 2-stage amplifier, with a high-frequency feedforward path. As such, it combines the high DC gain of a 2-stage and the large bandwidth of a single-stage amplifier.

The system of Fig. 13.1.1 is realized in a baseline 90nm CMOS process (Fig. 13.1.7). The chip area of the ΣΔ modulator is $0.5mm^2$. The measured spectra in this paper are of the digital output data Yi+jYq (see Fig. 13.1.1) before the decimation filter QDF. The sampling frequency is 340MHz and the total power consumption of the ΣΔ modulator including the QNCF is 56mW from a 1.2V supply. A 2-channel differential waveform generator is used to generate the quadrature input signals. Figure 13.1.4 shows the measured in-band output spectrum for a full-scale (FS) sinusoidal input tone at +1MHz with differential amplitude of 1V. The linearity is mainly limited by the mismatch between the unit elements of the DACs and can be further improved by using dynamic element-matching techniques. The measured SFDR is 80dB. This measurement demonstrates the capacitor matching in the feedback DACs. Figure 13.1.5 shows the measured IR with an input tone at –1MHz. The image at +1MHz is 58dB down. Other measured samples reveal similar results. From Fig. 13.1.5, it can be seen that the quantization noise in the negative image band is at maximum 40dB higher than the thermal noise level in the positive signal band. Hence, considering the high IR, there is no need for additional noise suppression in the negative image band, as noise leakage from the image band into the signal band is not a problem. This is usually needed in quadrature bandpass ΣΔ modulators [4] that have much higher quantization noise in the image band. Figure 13.1.6 presents the measured SNR as a function of the input signal amplitude (+1MHz). When the generator is disconnected from the input, the total integrated noise is –77dBFS in the 20MHz signal band at +10.5MHz IF, resulting in a DR of 77dB. When the signal generator is connected to the input nodes of the ΣΔ modulator, the noise level increases by 2dB, even in the case when no input signals are programmed. From Fig. 13.1.6, it can be observed that for small input signals, the noise level is limited to –75dBFS, due to the generator noise. At large input signal levels, the noise floor raises, as quantization noise folds back in the signal band due to non-linearity. The peak SNR is 71dB and the peak SNDR is 69dB. The FOM of the ΣΔ modulator is 0.2pJ/conversion step.

References:
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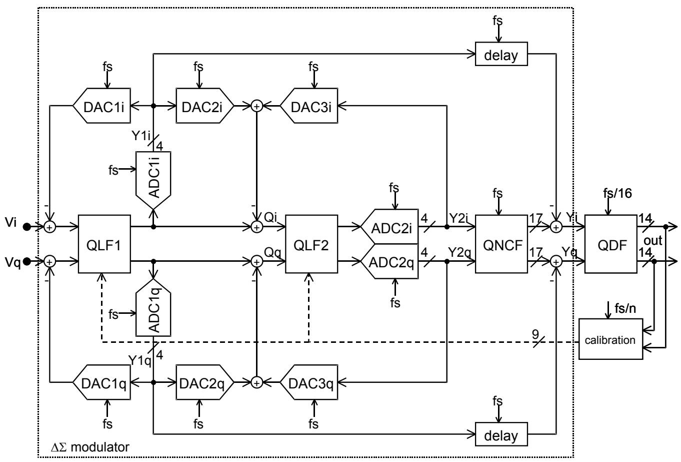

Figure 13.1.1: ADC architecture.

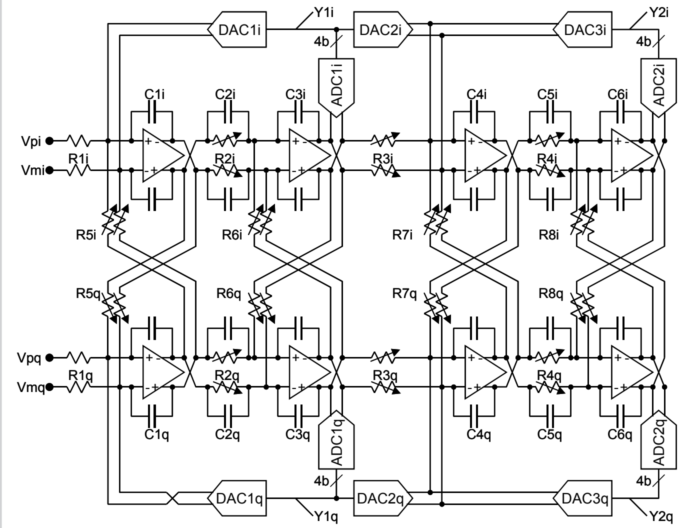

Figure 13.1.2: ΣΔ modulator design.

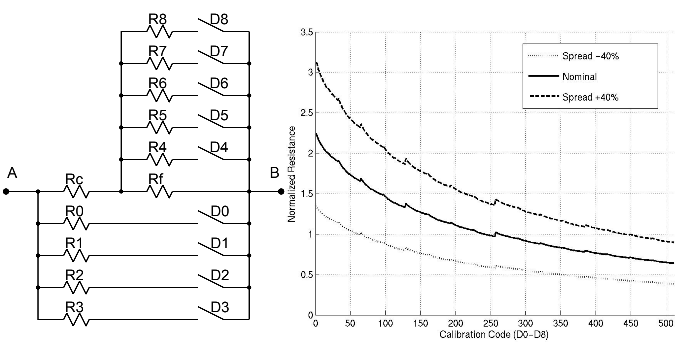

Figure 13.1.3: Programmable resistor schematic.

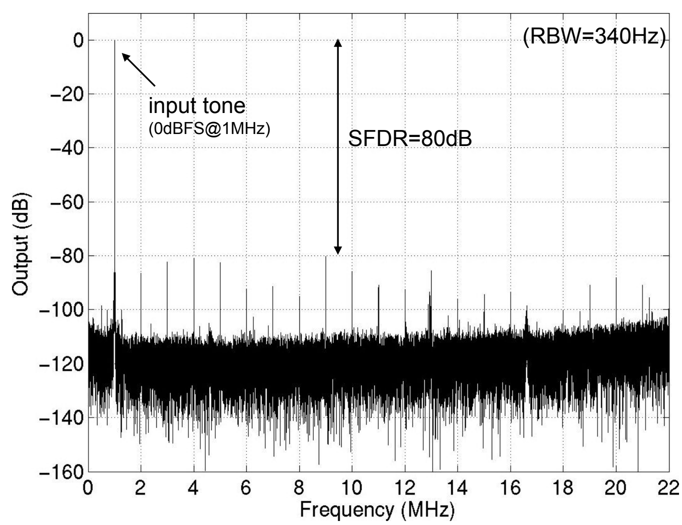

Figure 13.1.4: Fullscale input signal measurement.

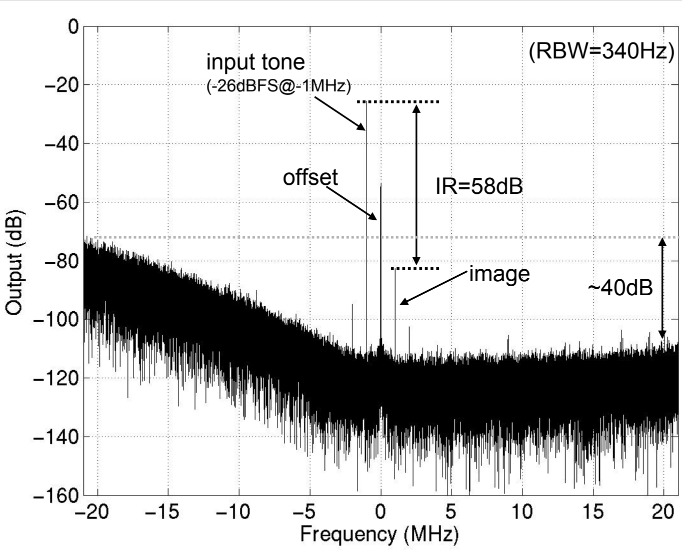

Figure 13.1.5: Image rejection measurement.

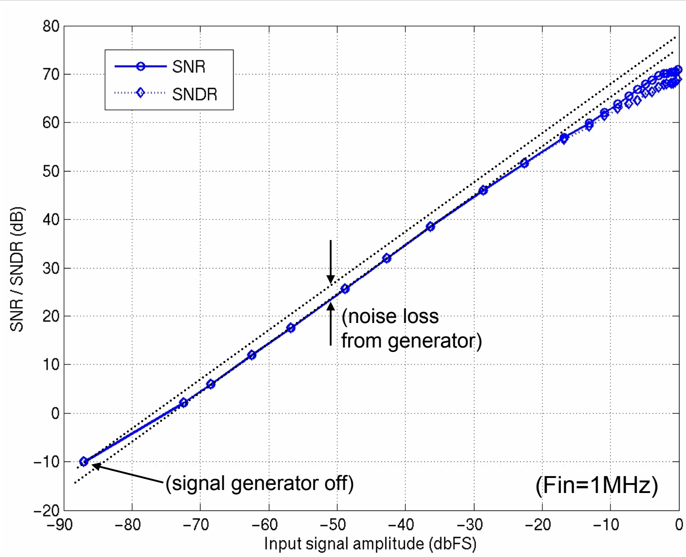

Figure 13.1.6: Measured SNR/SNDR versus input signal amplitude.

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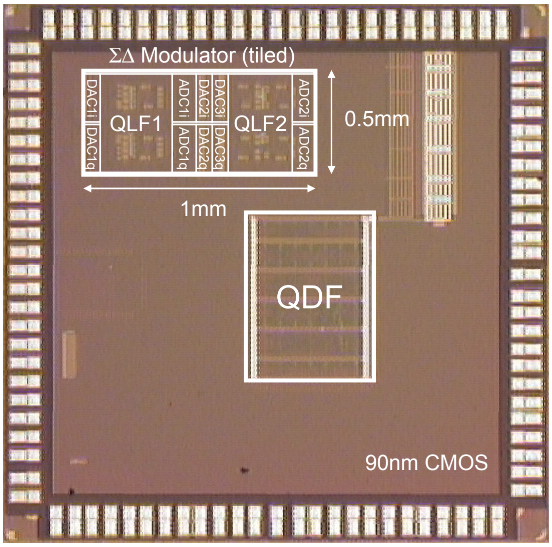

Figure 13.1.7: Chip micrograph.

